

(g) imagewise removing a portion of the photoresist from the top of the inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the inorganic dielectric layer;

(h) removing part of the inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the inorganic dielectric layer;

(i) removing the balance of the photoresist from the top of the inorganic dielectric layer and from the vias;

(j) filling the vias in the organic dielectric and the trenches in the inorganic dielectric with a metal.

8. (Amended) The integrated circuit structure [process] of claim 7 wherein steps (b) through (j) are repeated at least once on the previously formed integrated circuit structure.

11. (Amended) [A process for producing an] An integrated circuit structure produced by a process which comprises

(a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic via level dielectric on the substrate;

(c) depositing an thin inorganic dielectric layer on the organic via level dielectric;

(d) imagewise patterning and removing a portion of the thin inorganic dielectric layer thus defining vias through the thin inorganic dielectric layer;

(e) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer and filling the vias in the thin inorganic dielectric layer with the organic dielectric material;

(f) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;

(g) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form trenches in the metal level inorganic dielectric layer;

(h) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portion of the metal level inorganic dielectric to form trenches therein, and removing the organic etchstop material from the vias in the thin inorganic dielectric layer;

(i) removing the portion of the organic via level dielectric layer underlying the thin inorganic dielectric layer thus forming vias through the organic via level dielectric layer down to the metal lines;

(j) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

12. (Amended) The integrated circuit structure [process] of claim 11 wherein steps (b) through (j) are repeated at least once on the previously formed integrated circuit structure.

15. (Amended) [A process for producing an] An integrated circuit structure produced by a process which comprises

(a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic via level dielectric layer on the substrate;

(c) depositing an thin inorganic dielectric layer on the organic via level dielectric;

(d) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer;

(e) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;


(f) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form vias in the metal level inorganic dielectric layer;

(g) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portions of the metal level inorganic dielectric layer to form vias in the organic dielectric etchstop material layer;

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- (h) removing the portion of the thin inorganic dielectric layer underlying the corresponding removed portions of the organic dielectric etchstop material layer to form vias in the thin inorganic dielectric layer;
- (i) covering the top of the metal level inorganic dielectric layer with a photoresist and filling the vias in the metal level inorganic dielectric layer, the organic dielectric etchstop material layer and the thin inorganic dielectric layer with photoresist;
- (j) imagewise patterning and removing a portion of the photoresist from the top of the metal level inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the metal level inorganic dielectric layer;
- (k) removing part of the metal level inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the metal level inorganic dielectric layer;
- (l) removing the balance of the photoresist from the top of the metal level inorganic dielectric layer and from the vias; and removing the portion of the organic dielectric etchstop material layer underlying the trenches until the thin inorganic dielectric layer is reached;
- (m) removing the portion of the organic via level dielectric layer underlying the vias in the thin inorganic dielectric layer;
- (n) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

16. (Amended) The integrated circuit structure [process] of claim 15 wherein steps (b) through (n) are repeated at least once on the previously formed integrated circuit structure.

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19. (Amended) [A process for producing an] An integrated circuit structure produced by a process which comprises
- (a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

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- (b) depositing an organic via level dielectric layer on the substrate;
- (c) depositing an thin inorganic dielectric layer on the organic via level dielectric
- (d) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer;
- (e) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;
- (f) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form vias in the metal level inorganic dielectric layer;
- (g) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portions of the metal level inorganic dielectric layer to form vias in the organic dielectric etchstop material layer;
- (h) removing the portion of the thin inorganic dielectric layer underlying the corresponding removed portions of the organic dielectric etchstop material layer to form vias in the thin inorganic dielectric layer;
- (i) removing the portion of the organic via level dielectric layer underlying the corresponding removed portions of the thin inorganic dielectric layer to form vias in the organic via level dielectric layer;
- (j) covering the top of the metal level inorganic dielectric layer with a photoresist and filling the vias in the metal level inorganic dielectric layer, the organic dielectric etchstop material layer, the thin inorganic dielectric layer and the organic via level dielectric layer with photoresist;
- (k) imagewise patterning and removing a portion of the photoresist from the top of the inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the metal level inorganic dielectric layer;
- (l) removing part of the metal level inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the metal level inorganic dielectric layer;
- (m) removing the balance of the photoresist from the top of the metal level inorganic dielectric layer and from the vias; and removing the portion of the organic dielectric